FIG. 1

CONVENTIONAL DESIGN PROCESS

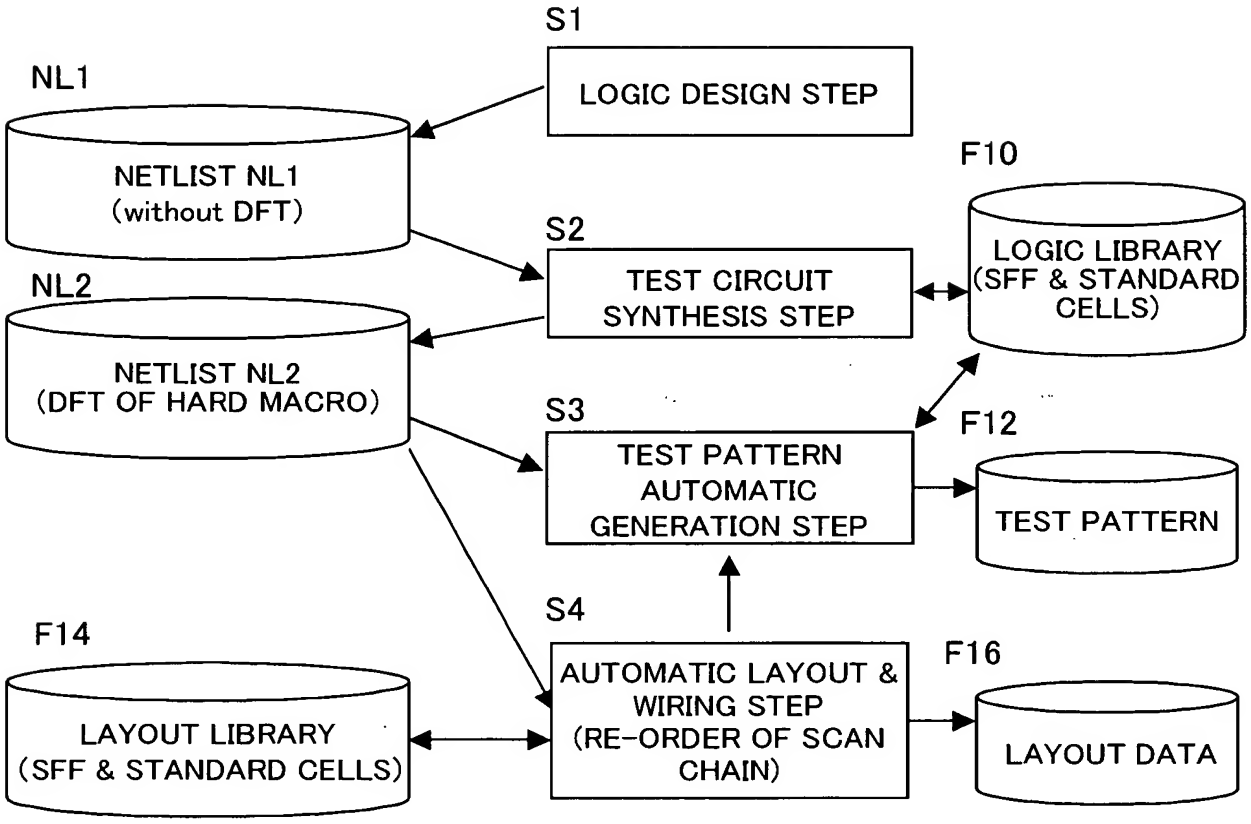


FIG. 2

COMPARATIVE EXAMPLE OF DESIGN PROCESS

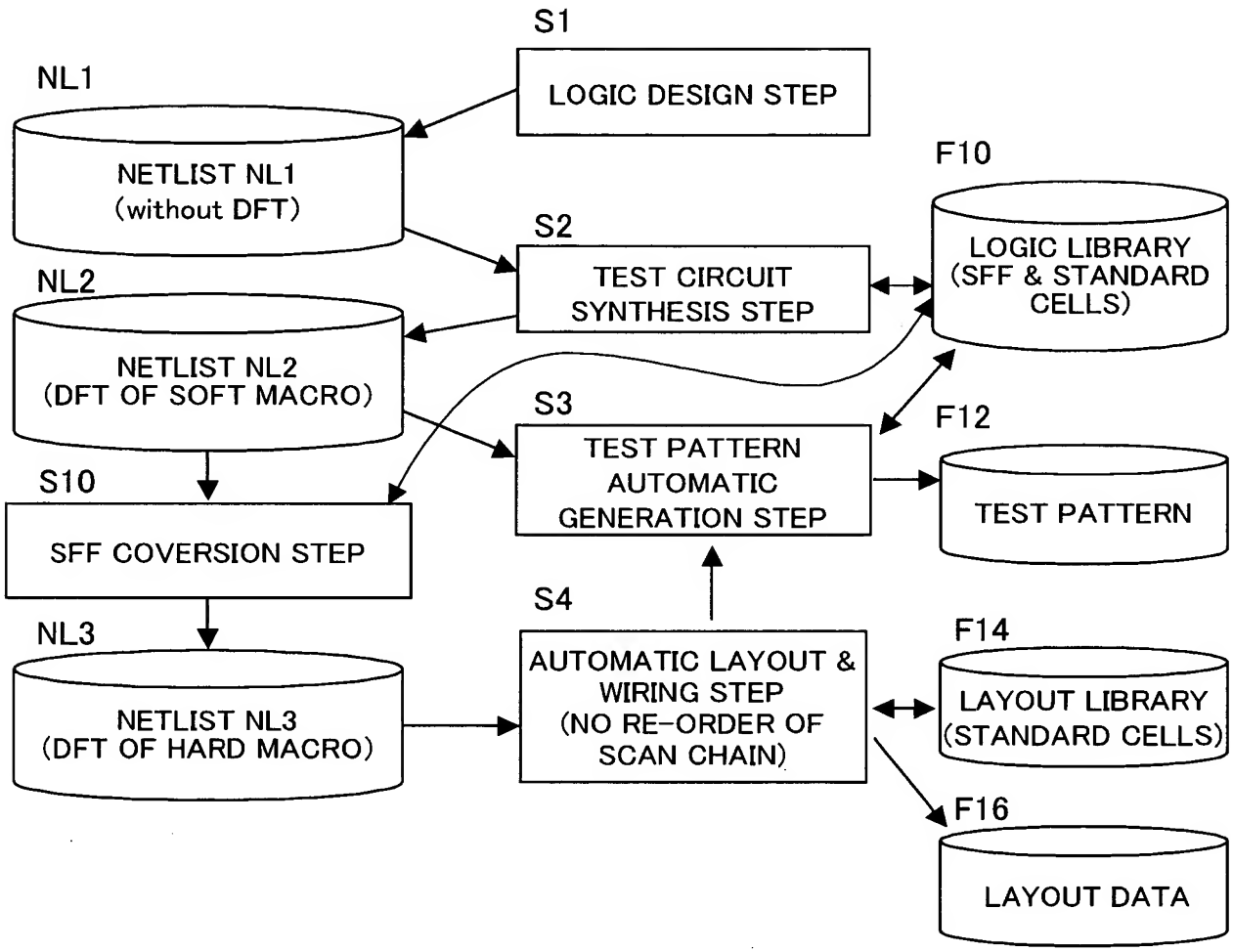


FIG. 3

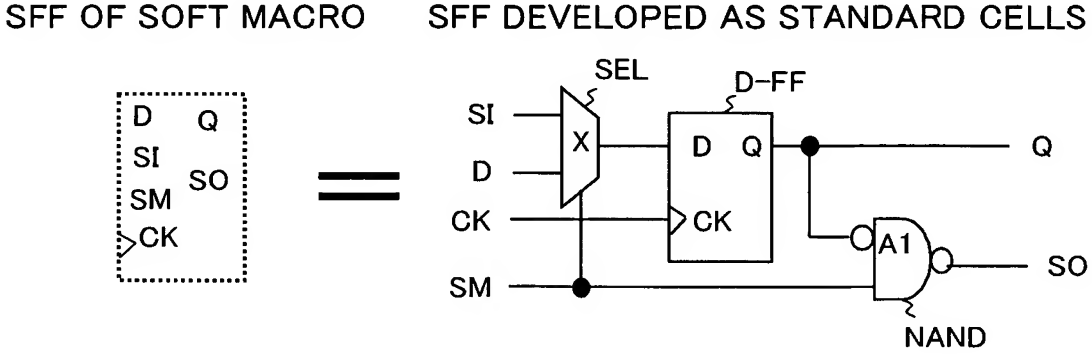


FIG. 4

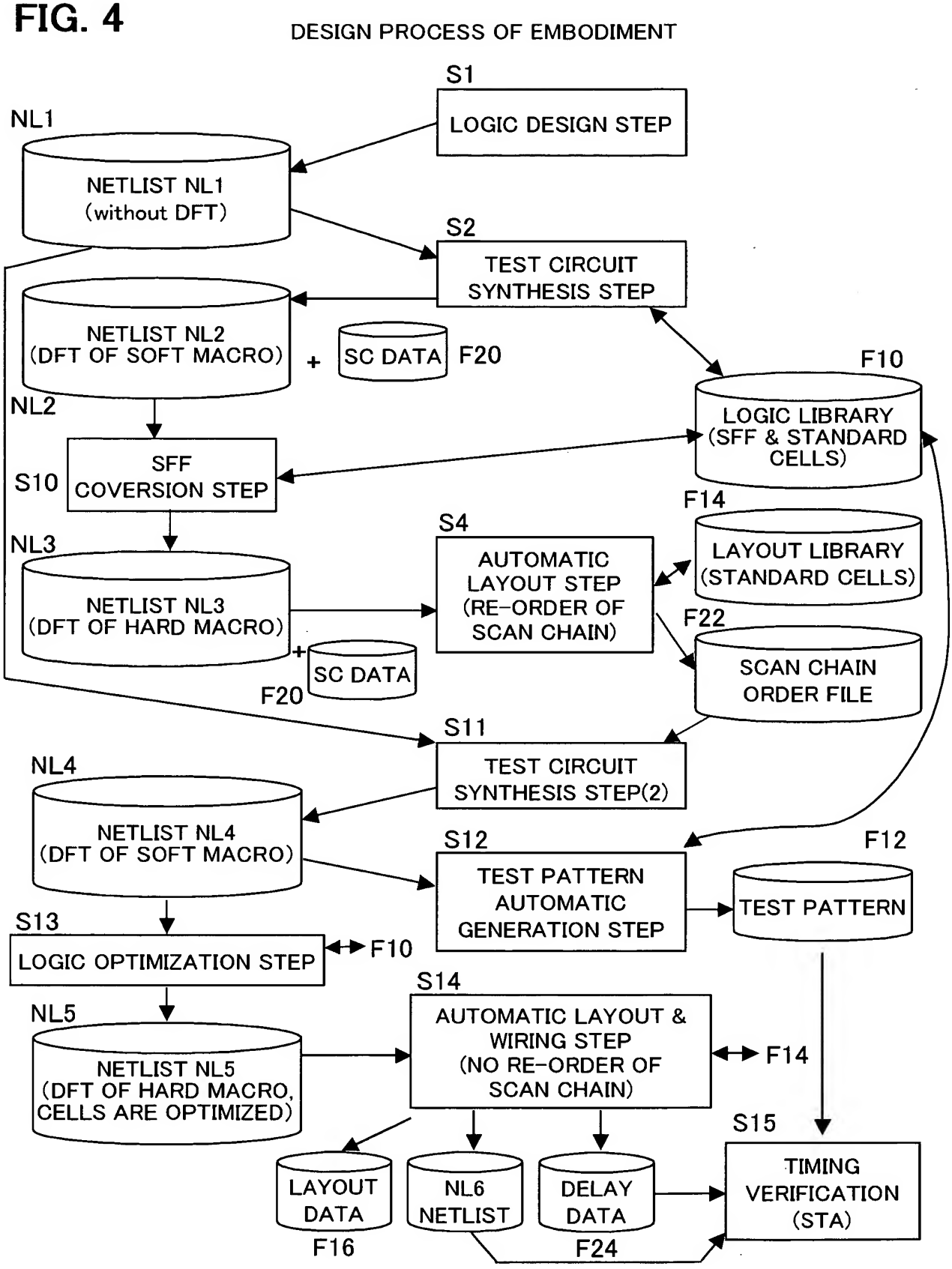

DESIGN PROCESS OF EMBODIMENT
S1
LOGIC DESIGN STEP
NL1
NETLIST NL1
(without DFT)
S2
TEST CIRCUIT
SYNTHESIS STEP
NETLIST NL2
(DFT OF SOFT MACRO)
+
SC DATA
F20
F10
LOGIC LIBRARY
(SFF & STANDARD
CELLS)
NL2
S10
SFF
COVERSION STEP
F14
LAYOUT LIBRARY
(STANDARD CELLS)
S4
NL3
AUTOMATIC
LAYOUT STEP
(RE-ORDER OF
SCAN CHAIN)
NETLIST NL3
(DFT OF HARD MACRO)
+
SC DATA
F20
F22
SCAN CHAIN
ORDER FILE
S11
TEST CIRCUIT
SYNTHESIS STEP(2)
NL4
NETLIST NL4
(DFT OF SOFT MACRO)
S12
F12
TEST PATTERN
AUTOMATIC
GENERATION STEP
TEST PATTERN
S13
LOGIC OPTIMIZATION STEP
F10
S14
NL5
AUTOMATIC LAYOUT &
WIRING STEP
(NO RE-ORDER OF
SCAN CHAIN)
F14
NETLIST NL5
(DFT OF HARD MACRO,
CELLS ARE OPTIMIZED)
S15
LAYOUT
DATA
NL6
NETLIST
DELAY
DATA
TIMING
VERIFICATION
(STA)
F16
F24

FIG. 5

NETLIST NL1

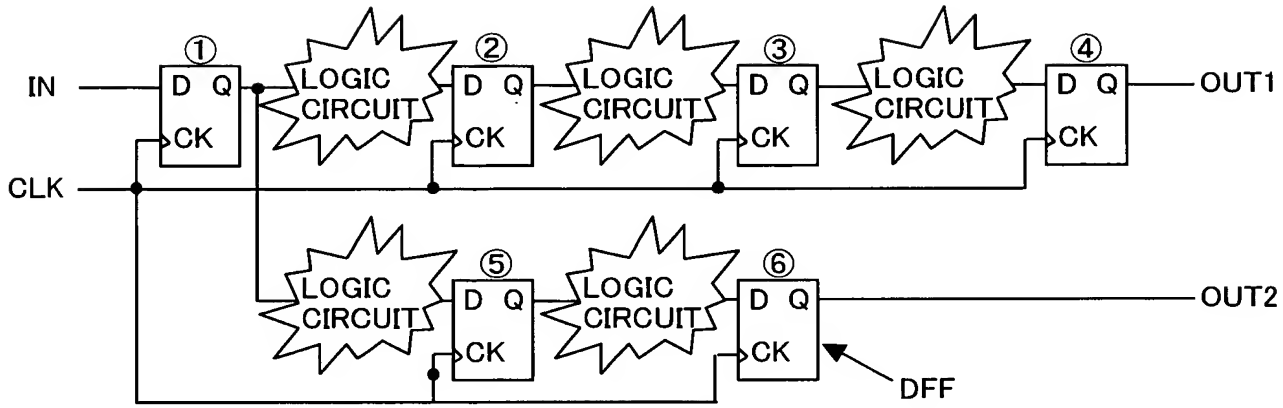


FIG. 6

NETLIST NL2

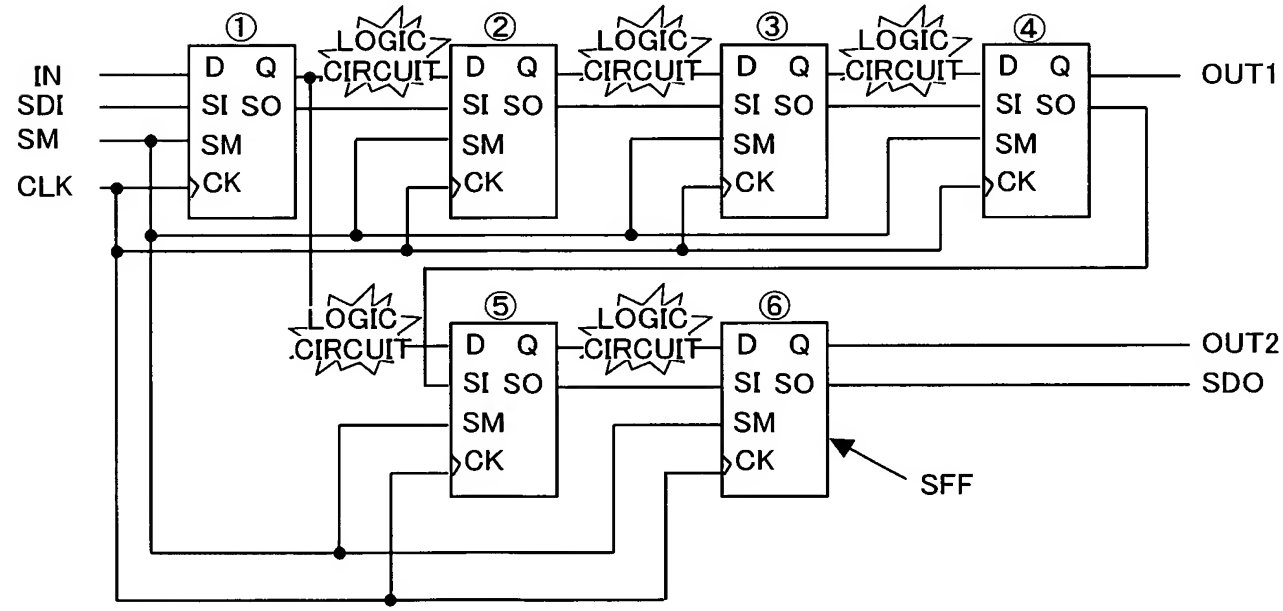


FIG. 7

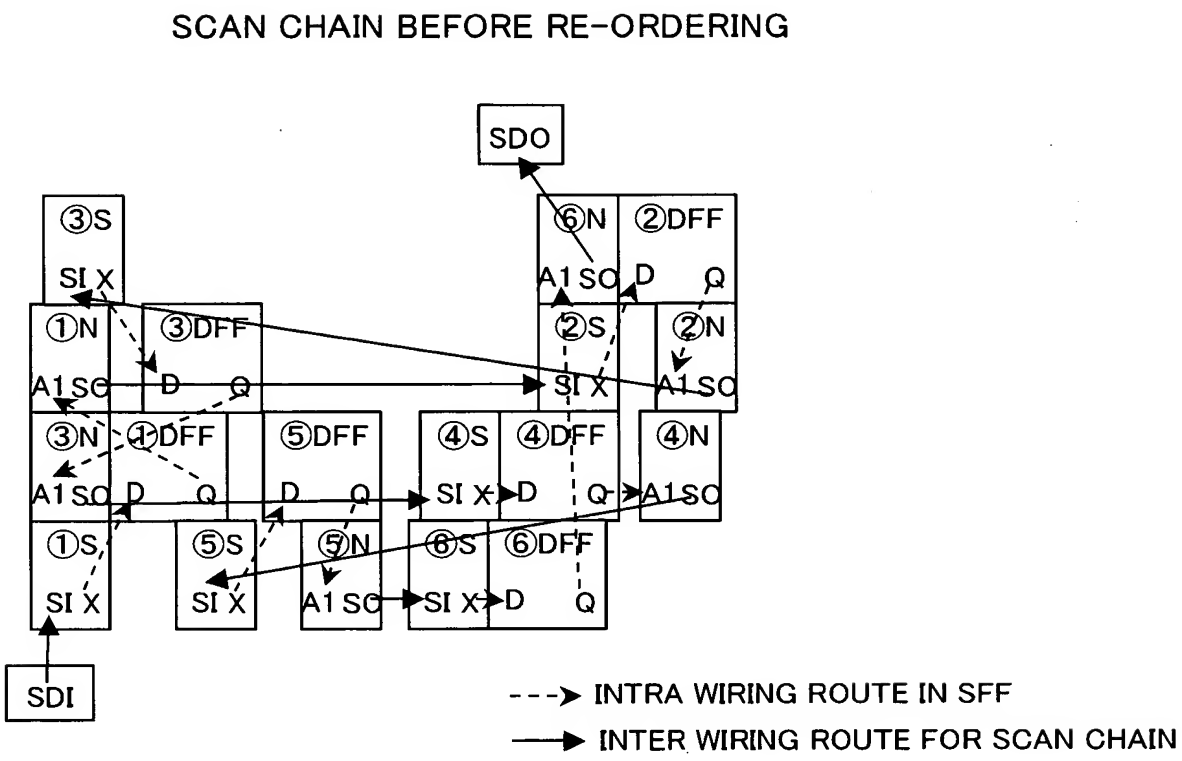

SCAN CHAIN BEFORE RE-ORDERING
SDO
③S
SI X
⑥N
A1 SO
②DFF
D
Q
①N
A1 SO
③DFF
D
Q
②S
SI X
②N
A1 SO
③N
A1 SO
①DFF
D
Q
⑤DFF
D
Q
④S
SI X
④DFF
D
Q
④N
A1 SO
①S
SI X
⑤S
SI X
⑤N
A1 SO
⑥S
SI X
⑥DFF
D
Q
SDI
---> INTRA WIRING ROUTE IN SFF
INTER WIRING ROUTE FOR SCAN CHAIN

FIG. 8

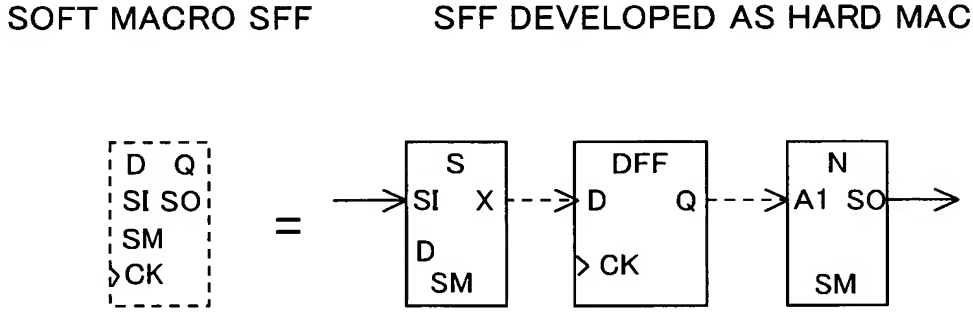

SOFT MACRO SFF
SFF DEVELOPED AS HARD MACROS
D Q
SI SO
SM
CK
=
S
SI X
D
SM
DFF
D Q
CK
N
A1 SO
SM

FIG. 9

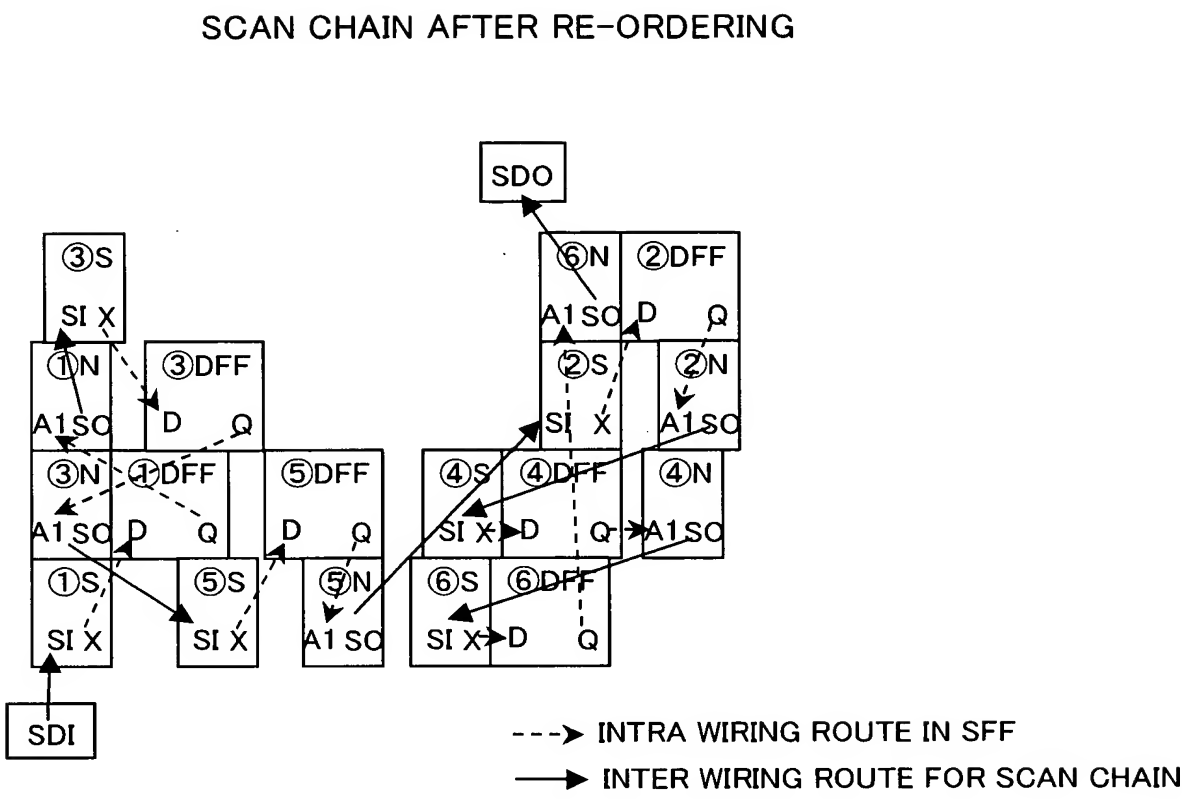
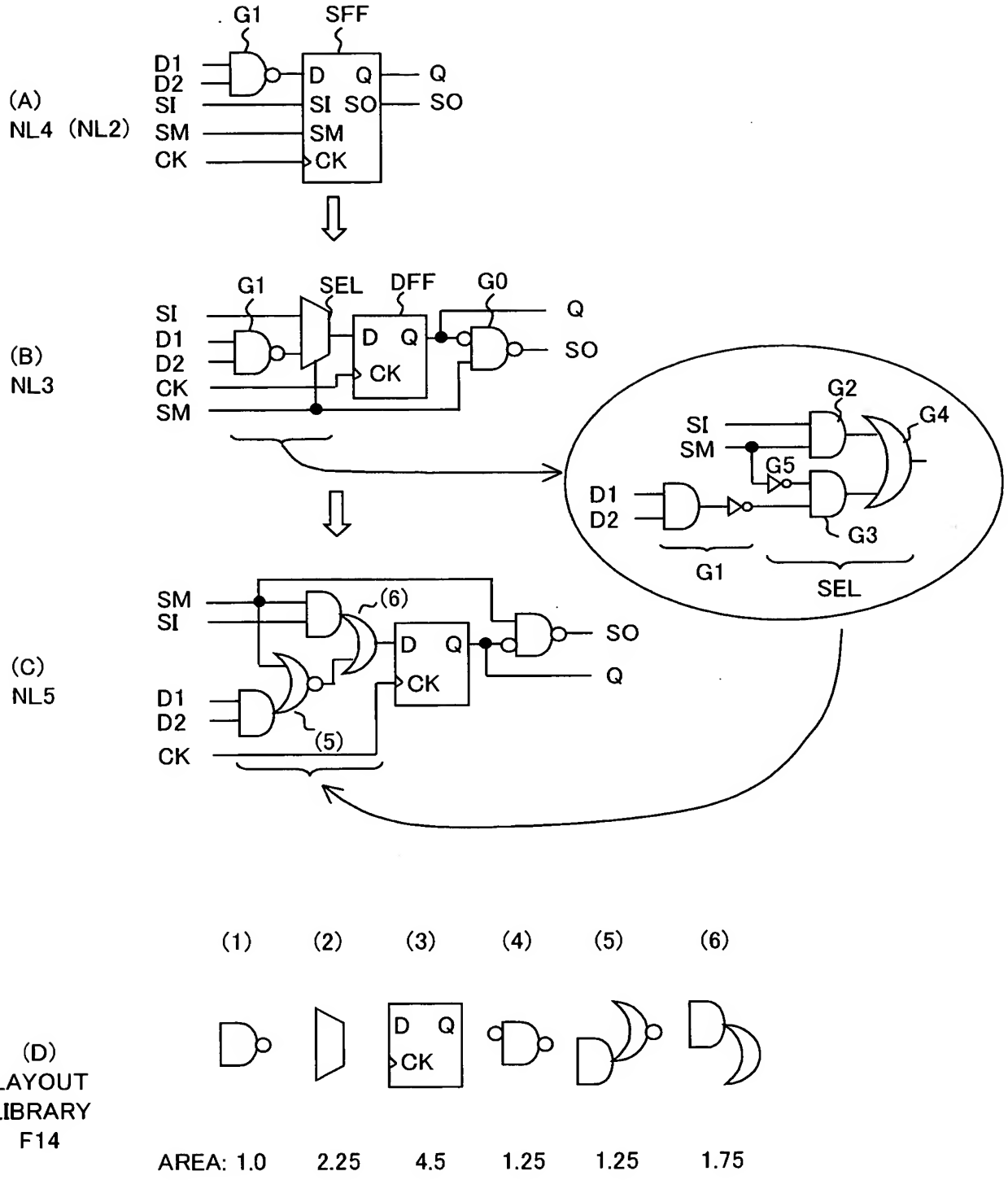

SCAN CHAIN AFTER RE-ORDERING
SDO
SDI
③S
SI X
①N
A1SO
③DFF
D Q
③N
A1SO
①DFF
D Q
①S
SI X
⑤S
SI X
⑤DFF
D Q
⑤N
A1SO
⑥N
A1SO
②DFF
D Q
②S
SI X
②N
A1SO
④S
SI X
④DFF
D Q
④N
A1SO
⑥S
SI X
⑥DFF
D Q
---> INTRA WIRING ROUTE IN SFF
INTER WIRING ROUTE FOR SCAN CHAIN

FIG. 10


(A)
NL4 (NL2)
G1
SFF
D1
D2
SI
SM
CK
D Q
SI SO
SM
CK
Q
SO
(B)
NL3
G1
SEL
DFF
G0
SI
D1
D2
CK
SM
D Q
CK
Q
SO
G2
G4
SI
SM
G5
D1
D2
G3
G1
SEL
(C)
NL5
SM
SI
(6)
D Q
CK
SO
Q
D1
D2
(5)
CK
(D)
LAYOUT
LIBRARY
F14
(1)
(2)
(3)
(4)
(5)
(6)
D Q
CK
AREA: 1.0
2.25
4.5
1.25
1.25
1.75